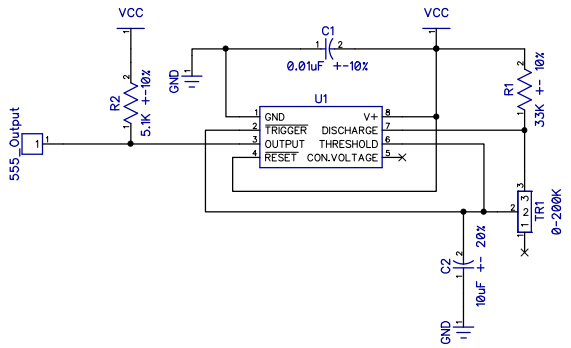
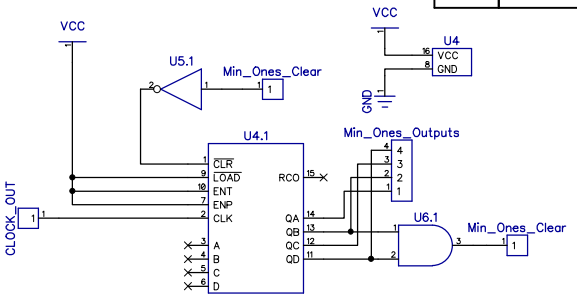
RevNo	Revision note	Date	Initials	Checked
1.0	Created schematic	5/07/2016	M.H	
1.1	Removed one LED decoder and replaced five decoders with BJTs	6/08/2016	M.H	
1.2	Added user clock interface	7/09/2016	M.H	

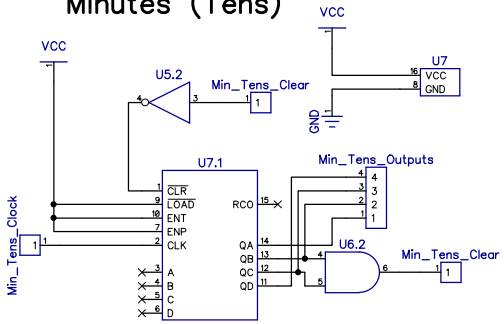
555 Timer



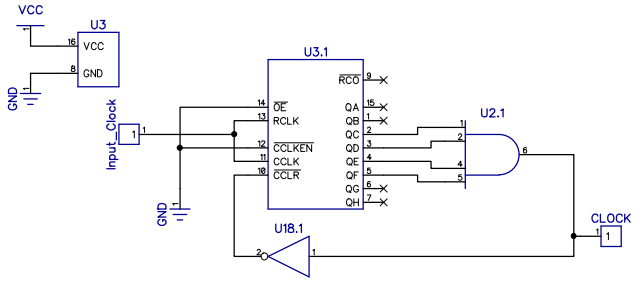
Minutes (Ones)



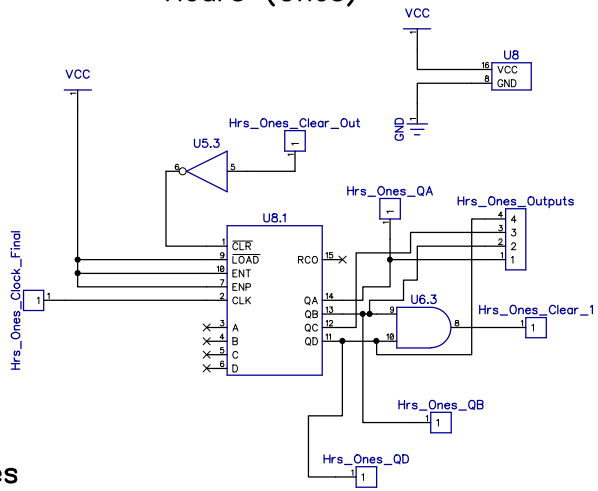
Minutes (Tens)



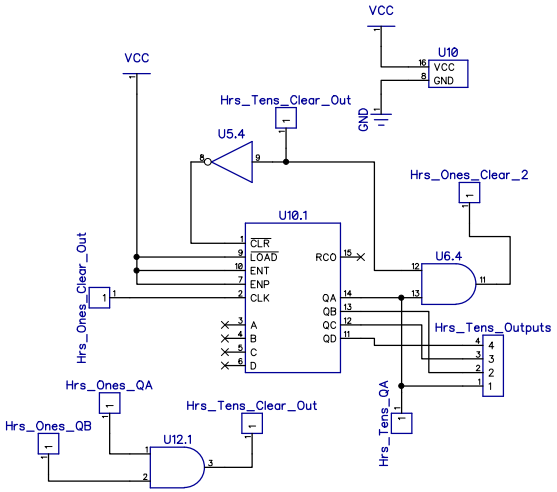
Input Counter (clock divide by 240)



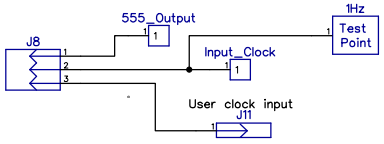
Hours (Ones)



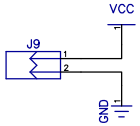
Hours (Tens)



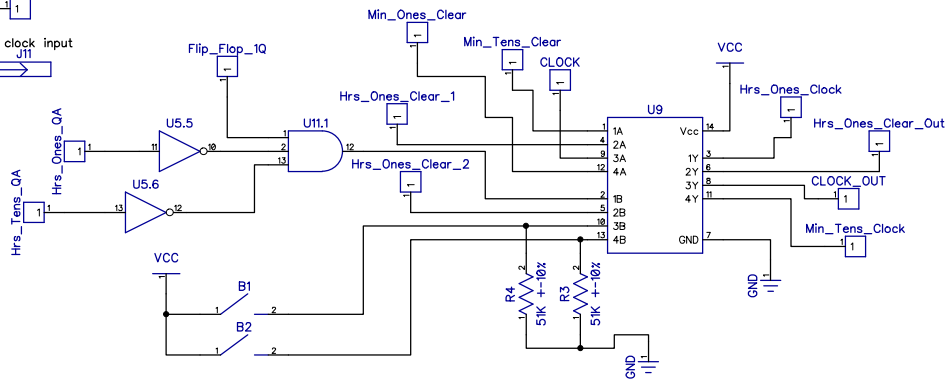
Clock Selection



Clock Power Jumper



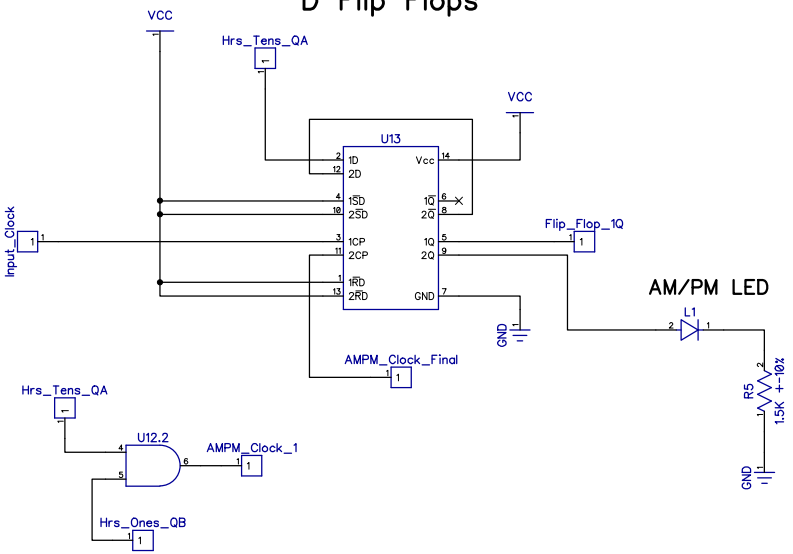
OR Gates



Title		
Sequential Logic Clock		
Size	Number	Rev
A3	EBESS-002-01	1.2
Date 5/07/2016	Drawn by M.Herbert	
Filename clock_schematics.dch	Sheet 1 of 4	

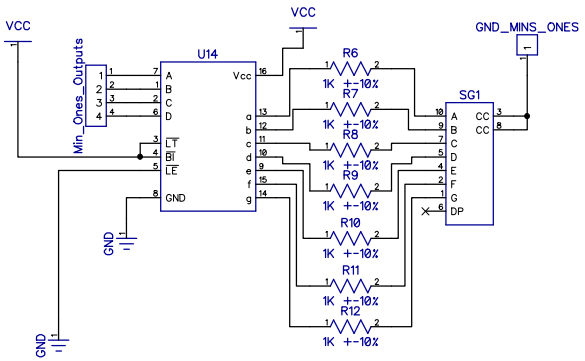
RevNo	Revision note	Date	Initials	Checked
1.0	Created schematic	7/07/2016	M.H	
1.1	Removed one LED decoder and replaced five decoders with BJTs	6/08/2016	M.H	
1.2	Fixed PM bug	7/09/2016	M.H	

D Flip Flops

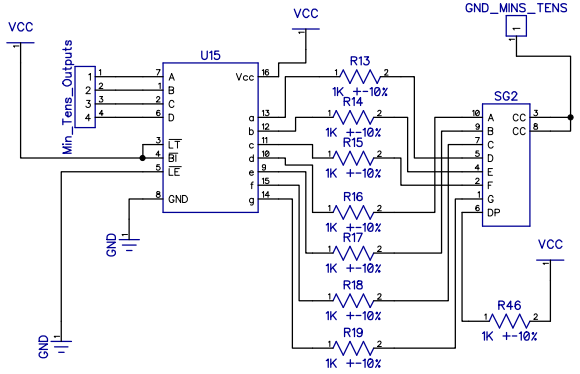


Seven Seg Displays

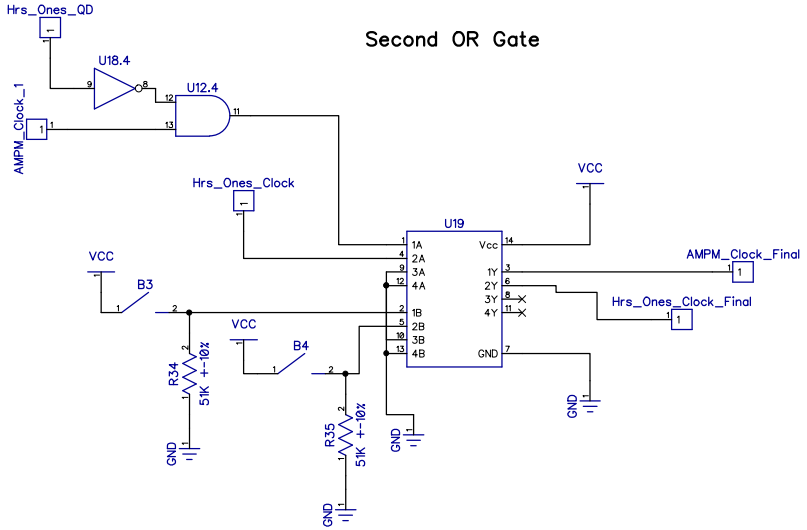
Minutes_Ones



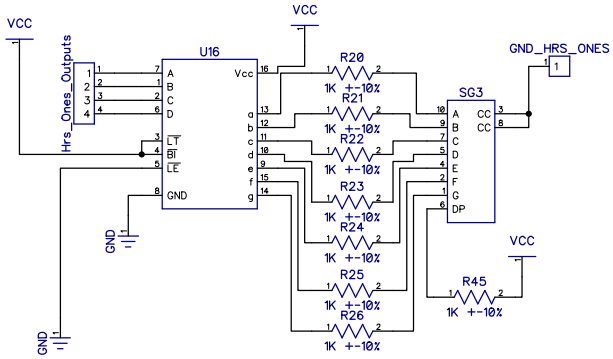
Minutes_Tens



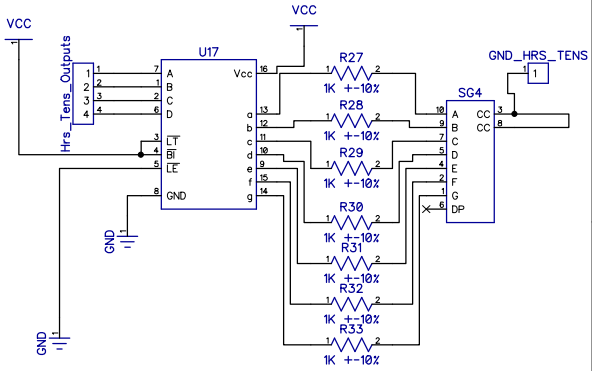
Second OR Gate



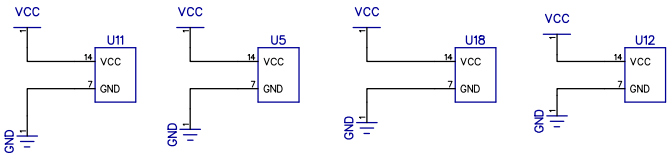
Hours_Ones

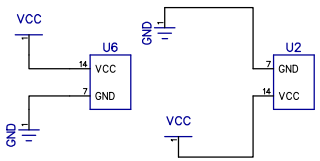


Hours_Tens



Power Rails

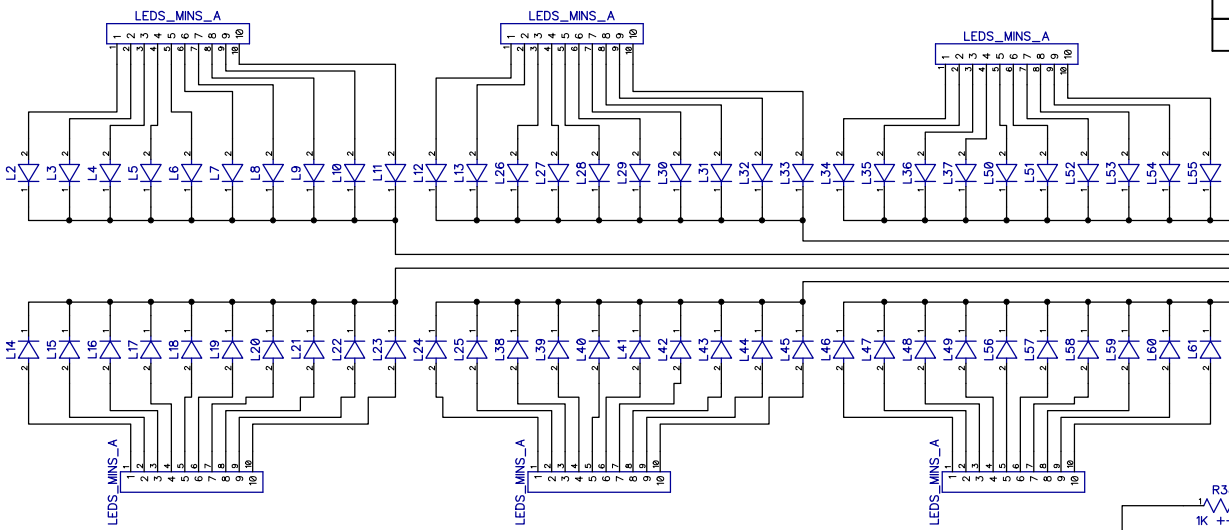




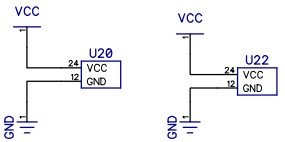
Title		
Sequential Logic Clock		
Size	Number	Rev
A3	EBESS-002-02	1.2
Date 7/07/2016	Drawn by M.Herbert	
Filename clock_schematics.dch	Sheet 2 of 4	

RevNo	Revision note	Date	Initials	Checked
1.0	Created schematic	8/07/2016	M.H	
1.1	Removed one LED decoder and replaced five decoders with BJTs	6/08/2016	M.H	
1.2	Changed emitter LED	7/09/2016	M.H	

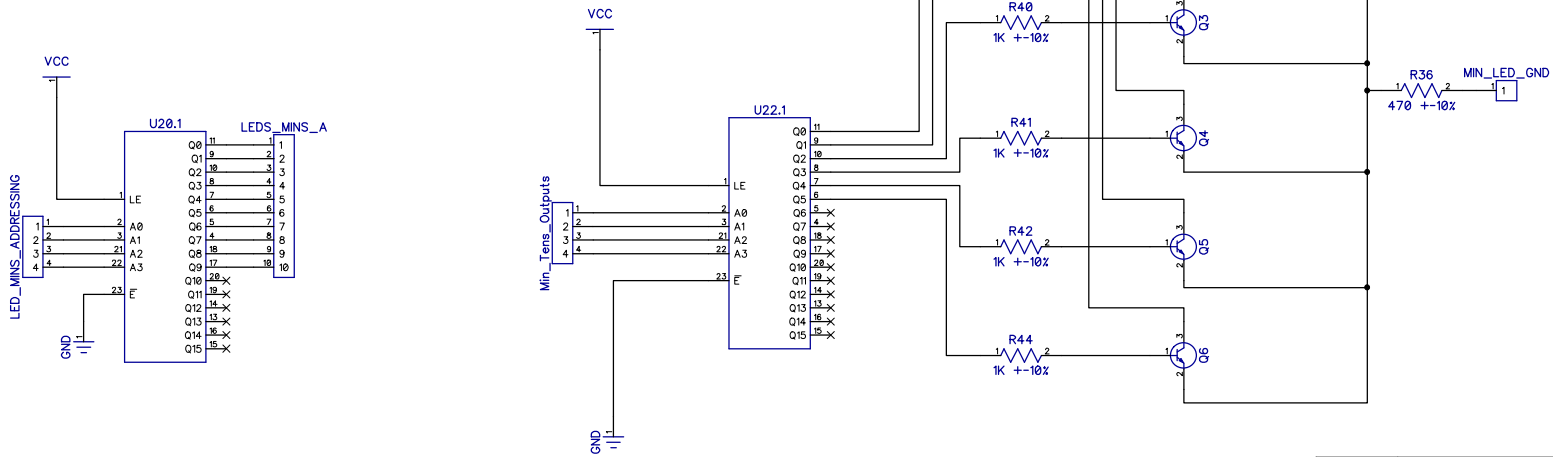
Minute LEDs



Power Rails



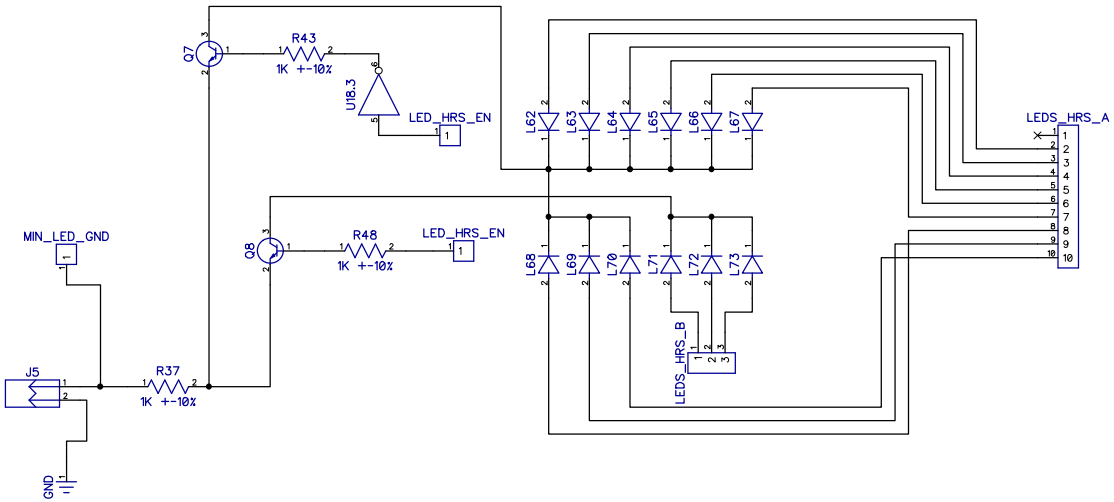
Decoders for Minute LEDs



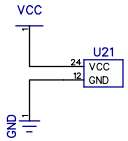
Title		
Sequential Logic Clock		
Size	Number	Rev
A3	EBESS-002-03	1.2
Date 6/08/2016	Drawn by M.Herbert	
Filename clock_schematics.dch	Sheet 3 of 4	

RevNo	Revision note	Date	Initials	Checked
1.0	Created schematic	11/07/2016	M.H	
1.1	Removed one LED decoder and replaced five decoders with BJTs	6/08/2016	M.H	
1.2	Fixed LED logic	7/09/2016	M.H	

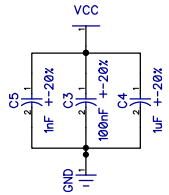
Hour LEDs

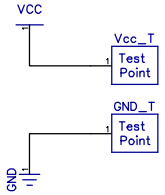


Power Rails



Decoupling Capacitors

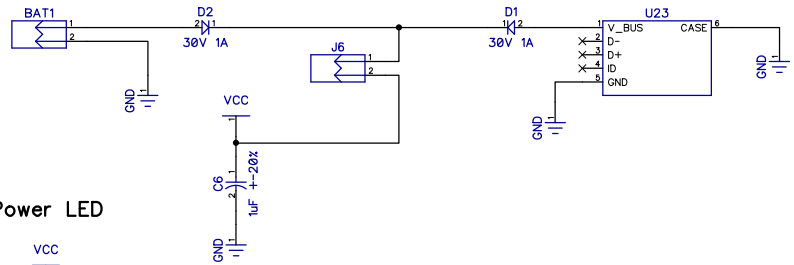


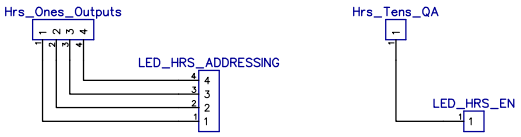


Battery Pack Power

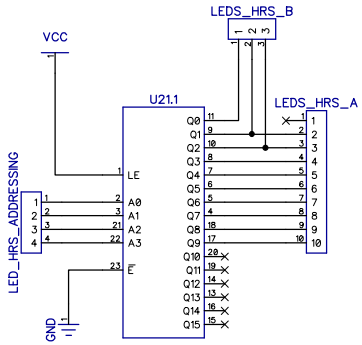
Power Switch

Micro USB-B Power

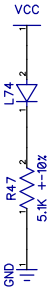




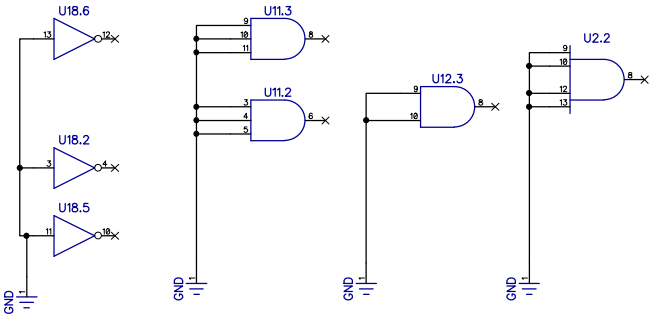
Decoder for Hour LEDs



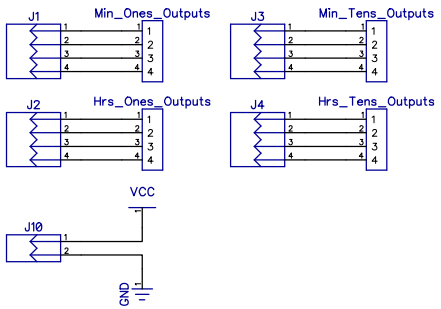
Power LED



Unused gates



Broken-out alarm pins



Title		
Sequential Logic Clock		
Size	Number	Rev
A3	EBESS-002-04	1.2
Date 6/08/2016	Drawn by M.Herbert	
Filename clock_schematics.dch	Sheet 4 of 4	